

BUTTON OPERATION

- 0-7 Input Register Entry
- EXAMINE** Display memory contents at current address
Successive presses increment current address
- DEPOSIT** Deposit Input Register to current address and increment current address
- STEP** Execute single instruction at current PC
- RUN/HALT** Begin or end freerun mode
- RESET** Halt CPU, set PC=0, clear all registers. 2nd press gives option to clear all memory.
- PROG LOAD** Arm system for memory load from external system via "upload" program.
- DISPLAY MODE** Switch among four different display modes.
- INTERRUPT** Push PSW and PC to stack
disable interrupts and call location 0376

SPECIAL REGISTERS

LOCATION	MEANING
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400	R0
401	R1
402	R2
403	R3
404	R4
405	R5
406	R6
407	R7
410	PC
411	PSW
412	SP

413-452 Stack Entries
(most recent at 413, then 414, 415, etc.)

771-774 Saved Prog 1-4

775-777 Shout outs and thank yous :)

Octal Conversion Table

ABC	0	1	2	3	4	5	6	7
00	0	1	2	3	4	5	6	7
01	8	9	10	11	12	13	14	15
02	16	17	18	19	20	21	22	23
03	24	25	26	27	28	29	30	31
04	32	33	34	35	36	37	38	39
05	40	41	42	43	44	45	46	47
06	48	49	50	51	52	53	54	55
07	56	57	58	59	60	61	62	63
10	64	65	66	67	68	69	70	71
11	72	73	74	75	76	77	78	79
12	80	81	82	83	84	85	86	87
13	88	89	90	91	92	93	94	95
14	96	97	98	99	100	101	102	103
15	104	105	106	107	108	109	110	111
16	112	113	114	115	116	117	118	119
17	120	121	122	123	124	125	126	127

000-177 octal=ABC
200-377
decimal shown in table

TOUCH METAL PROGRAMMER'S CARD



- 8-bit CPU, 256 bytes memory
- 8 general purpose registers
- 32-byte stack
- single interrupt vector
- 5 status bits
- 3 addressing modes
- (direct, indirect and immediate)



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INSTRUCTION FORMATS

CLASS	EXAMPLES
No operands	Halt, RTI
Opcode Address	Jump, Call
Opcode src, dst	Add R2, R3 Add (R4), (R7)
Opcode reg, immed	LDI R2, 213
Opcode (reg), immed	LDI (R2), 213
Opcode reg	INC R2
Opcode (reg)	INC (R2)
s, d, r are each 3-bit numbers:	0=R0 1=R1 2=R2 3=R3 4=R4 5=R5 6=R6 7=R7

m is a 2-bit number, describing the access mode of the source and destination registers:

- 0=src, dst
- 1=src, (dst)
- 2=(src), dst
- 3=(src), (dst)

INSTRUCTION SUMMARY

INSTRUCTION	CODING	FLAGS
NOP	000	
RET	001	
HALT	002	
CALL address	003 aaa	
JMP address	004 aaa	
JZ address	005 aaa	
JNZ address	006 aaa	
JN address	007 aaa	
JNN address	010 aaa	
JC address	011 aaa	
JNC address	012 aaa	
JV address	013 aaa	
JNV address	014 aaa	
ADD src, dst	020 msd	VCNZ
SUB src, dst	021 msd	VCNZ
MUL src, dst	022 msd	VCNZ
DIV src, dst	023 msd	VCNZ
AND src, dst	024 msd	NZ
OR src, dst	025 msd	NZ
XOR src, dst	026 msd	NZ
MOV src, dst	027 msd	NZ

aaa is an 8-bit address
msd specifies mode/src/dst

INSTRUCTION SUMMARY

INSTRUCTION	CODING	FLAGS
IntE	030	
IntD	031	
RTI	032	
LDI reg, value	07r iii	
INC reg	10r	CNZ
DEC reg	11r	CNZ
CLR reg	12r	
NOT reg	13r	NZ
ROL reg	14r	CNZ
ROR reg	(C is the old bit 7)	
IN reg	15r	CNZ
OUT reg	(C is the old bit 0)	
LDI (reg), value	16r	NZ
INC (reg)	17r	
DEC (reg)	27r iii	
CLR (reg)	30r	CNZ
NOT (reg)	31r	CNZ
ROL (reg)	32r	
ROR (reg)	33r	NZ
IN (reg)	34r	CNZ
OUT (reg)	(C is the old bit 7)	
LDI (reg), value	35r	CNZ
INC (reg)	(C is the old bit 0)	
DEC (reg)	36r	NZ
CLR (reg)	37r	
NOT (reg)		
ROL (reg)		
ROR (reg)		
IN (reg)		
OUT (reg)		

iii is an 8-bit immediate value